

REMARKS


This response is to the Office Letter mailed in the above-referenced case on November 19, 2002, being a first action and non-Final. Claims 1-24 are standing for examination. In the Office Letter the Examiner has rejected claims 1-24 under 35 U.S.C. 103(a) as being unpatentable over Rosenthal et al., (US 5,918,050), hereinafter Rosenthal.

In response to the Examiner's rejections and comments, applicant herein provides arguments to more particularly point out the non-obvious subject matter regarded as inventive by applicant and to unarguably distinguish applicant's invention over the art of Rosenthal presented by the Examiner. Claims 7 and 13 are herein amended to correct language only.

Regarding claims 1, 7, 13 and 18, the Examiner states Rosenthal discloses a background memory manager (BMM) (MMU, 50, 52+DMA, 35 within I/O control Unit, 29, Fig. 4) for managing memory in a data processing system, the BMM comprising circuitry for transferring data to and from an outside device and to and from a memory, a memory state map associated with the memory and a communication link to a processor (21, Fig. 2).

The Examiner continues to state that because Rosenthal teaches a BMM that manages memory it would be obvious that Rosenthal's BMM would perform the inherent characteristics of a BMM. Particularly, the Examiner states, the BMM would obviously determine if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location. (abstract, col. 6, lines 58-col. 26).

Applicant respectfully points out that applicant's claims very specifically recite functions of a BMM. Applicant would appreciate it if the Examiner could be more specific when referencing a portion of art than to refer to a block of 20



columns to support the rejection of specific limitations in applicant's claims.


Applicant argues that the art of Rosenthal teaches an I/O Control Unit 29, which primarily serves as a buffer between outside devices and an operating system. The primary feature of unit 29 is FIFO unit 31 (buffer) for receiving incoming commands addressed to the I/O devices on device bus 34.

Rosenthal discloses that the input/output architecture has been designed so that it eliminates almost all operations which read registers of input/output devices. In order to accomplish this, the input/output control unit includes a first-in first-out (FIFO) unit for storing instructions directed to the input/output control unit. The FIFO unit queues incoming write operations; but, unlike FIFO units used in prior art systems, it stores both addresses and data. This allows the write operations to the input/output control unit to occur asynchronously so that both the central processing unit and the input/output control unit may be functioning independently of one another and neither need wait for operations of the other.

Applicant points out that Rosenthal's unit 29 includes DMA 35, but applicant argues, DMA 35, nor any other element of Rosenthal is taught to serve the functions of the BMM as disclosed and claimed in applicant's invention.

Rosenthal teaches that the input/output control unit also includes an advanced direct memory access (DMA) device to assist data transfers involving input/output devices associated with the input/output control unit. The DMA device allows the results of input/output operations to be written by input/output devices to main memory rather than requiring read operations by the central processing unit to obtain these results as in prior art systems. This eliminates almost all need for the central processing unit to read input/output devices and drastically increases the overall speed of input/output operations.

Applicant argues that the DMA of Rosenthal only saves the processing unit from having to read operations and obtain results for memory by allowing the I/O device to write directly to memory. Applicant's independent claims 1 and 7 clearly recite determining if each data structure fits into the memory, deciding exactly




where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location. Applicant argues that the functions of applicant's claims are far more limiting than the teachings of Rosenthal, and therefore are patentable unless Rosenthal (or another prior art reference) teaches these functions.

Applicant points out in the "background" portion of the present application that there are in the state-of-the-art two well-known mechanisms to bring data into the memory and send it out to a device when necessary. One mechanism is loading and storing the data through a sequence of Input/Output (I/O) instructions. The other is through a direct-memory access device (DMA).

In the case of a sequence of I/O instructions, the processor spends significant resources in explicitly moving data in and out of the memory. In the case of a DMA system, the processor programs an external hardware circuitry to perform the data transferring. The DMA circuitry performs all of the required memory accesses to perform the data transfer to and from the memory, and sends an acknowledgement to the processor when the transfer is completed.

In both cases of memory management in the art the processor has to explicitly perform the management of the memory, that is, to decide whether the desired data structure fits into the available memory space or does not, and where in the memory to store the data. To make such decisions the processor needs to keep track of the regions of memory wherein useful data is stored, and regions that are free (available for data storage).

Applicant argues that the unit 29 of Rosenthal, including its components is not capable of managing the memory as disclosed and claimed in applicant's invention. The unit 29 of Rosenthal may allow I/O devices to write directly to memory, but the intricate management of memory as disclosed and claimed in applicant's invention is still provided by the processing unit of Rosenthal. There is no disclosure of Rosenthal stating otherwise. Therefore, applicant's invention




clearly has a patentable novelty over the art of Rosenthal. Further, applicant points out that because the unit 29 of Rosenthal allows I/O devices to write directly to memory, the level of memory control exercised by the BMM as claimed in applicant's invention would not be possible. Applicant argues that one with skill in the art would not look to a system which allows I/O devices to write directly to memory when contemplating an invention for managing the internal memory as disclosed and claimed in applicant's invention, because the writing process could not be adequately controlled by the BMM.

Applicant points out to the Examiner that in order to support the conclusion that the claimed invention is directed to obvious subject matter, either the reference must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious **in light of the teachings of the reference.** Both the suggestion to make the claimed combination and the reasonable expectation of success must be founded in the prior art and not in applicant's disclosure. Applicant argues that the concept of determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location are only suggested in applicant's specification, not the art of Rosenthal. Rosenthal has absolutely no disclosure for managing internal aspects of memory 23.

Applicant believes claims 1, 7, 13, and 18 are clearly patentable as argued above. Claims 2-6, 8-12, 14-17, and 19-24 are clearly patentable on their own merits as argued above.

In view of the above amendments, and remarks, it is clear that the present case is now completely allowable. It is therefore respectfully requested that this application be reconsidered, the claims be allowed, and that this case be passed quickly to issue.

If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are



any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

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Version With Markings to Show Changes Made

7. (Amended) A data processing system, comprising:

a processor;

a memory coupled to the processor; and

a background memory manager (BMM) coupled to the memory and the processor, the background memory manager including circuitry for transferring data to and from an outside device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

13. (Amended) A network packet router, comprising:

an input/output (I/O) device for receiving and sending packets on the network;

a processor;

a memory coupled to the processor; and


a background memory manager (BMM) coupled to the memory and the processor, the background memory manager including circuitry for transferring packets to and from the I/O device and to and from the memory, and a memory state map associated with the memory;

characterized in that the BMM manages the memory, determining if each



data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

Respectfully Submitted,
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